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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/540,334	06/20/2005	Pierre Gidon	034299-650	8704

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EXAMINER	
MANDALA, VICTOR A	
ART UNIT	PAPER NUMBER
2826	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/13/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

T. H

Office Action Summary	Application No.	Applicant(s)	
	10/540,334	GIDON, PIERRE	
	Examiner	Art Unit	
	Victor A. Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/17/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

1. Claim 13 and 14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 13 recites the limitation of different nature and the examiner is unsure what the limitation is trying to limit the claim from. Is nature the type of material or crystallinity, or size, or location? Claim 14 recites the limitation of restore, where the examiner is unsure what is meant by this limitation. Restore what? Claim 14 also recites the limitation of until so on, where the examiner is also unsure what is meant by this limitation. Until so on what?

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,465,860 Shigenaka et al.

2. Referring to claim 1, Shigenaka et al. teaches a matrix structure of multispectral detectors comprising: a superimposition of several layers of semiconductor material, (Figure 6 #31, 12, &

15 and Col. 8 Line 15), separated by layers of dielectric material, (Figure 6 #13 and Col. 8 Line 17), transparent to a light to be detected, (Col. 8 Line 10 and where the claim does not teach a narrower definition of what the spectrum of light includes such as visible light), said superimposition offering a face for receiving the light to be detected, (Figure 6 #11), said superimposition of layers of semiconductor material being spread out in picture elements or pixels, (Col. 3 Lines 42-51), each part of the layer of semiconductor material, (Figure 6 #31, 12, & 15), corresponding to a pixel comprising a light detection element, (Figure 6 #31, 12, 13 & 15), delivering electrical charges in response to the light received, (Col. 3 Lines 42-51), by said detection element, (Figure 6 #31, 12, 13 & 15), means for collecting the electrical charges delivered by each light detection element, (Figure 6 #31, 12, 13 & 15), said collection means, (Figure 4 #24 & 29), being electrically connected to electrical connection means, (Figure 6 #20, 24, & 34), and comprising conductive walls, (Figure 6 #21 & 33), filling trenches formed in the superimposition of layers of semiconductor material, (Figure 6 #31, 12, & 15), to assure an electrical contact with all of the layers of semiconductor material, (Figure 6 #31, 12, & 15), and to form an electrode, (Figure 4 #24), common to all of the detection elements, (Figure 6 #31, 12, 13 & 15).

3. Referring to claim 2, Shigenaka et al. teaches a structure according to claim 1, wherein it has the form of a wafer having two principal opposite faces: a first face that is the face for receiving the light to be detected, (Figure 6 #11), and a second face electrically insulated and supporting the electrical connection means, (Figure 6 #18).

4. Referring to claim 3, Shigenaka et al. teaches a structure according to claim 2, wherein second face constitutes a hybridization face with a device for exploiting the electrical charges

collected, (Figure 6 #18 is the face of the device where the electrical connections are located and where the device will be mated to another device or circuit board that will use or exploit the electrical charges collected).

5. Referring to claim 4, Shigenaka et al. teaches a structure according to claim 1, wherein the collection means comprise conductive feed throughs, (Figure 6 #20, 24, & 34).

6. Referring to claim 5, Shigenaka et al. teaches a structure according to claim 4, wherein the conductive feed throughs, (Figure 6 #20, 24, & 34), are lodged in sinks, (Figure 6 the via or opening around #20, 24, & 34), each sink having a depth that makes it possible to reach a corresponding detection element in crossing, (Figure 6 #31, 12, 13 & 15), without electrical contact, at least one of said layers of dielectric semiconductor material, (Figure 6 #31, 12, 13 & 15).

7. Referring to claim 6, Shigenaka et al. teaches a structure according to claim 1, wherein said element comprises at least one semiconductor detection junction, (Figure 6 #31, 12, 15 & 32).

8. Referring to claim 7, Shigenaka et al. teaches a structure according to claim 6, wherein said semiconductor junction is constituted by the presence of a doped zone in said part of the layer of semiconductor material, (Figure 6 #32 & Col. 8 Line 32).

9. Referring to claim 8, Shigenaka et al. teaches a structure according to claim 1, wherein the trenches are formed along a network of arrays such that an array contains several detection elements, (Col. 3 Lines 42-51 teaches a matrix of the elements as shown in Figure 6).

10. Referring to claim 9, Shigenaka et al. teaches a structure according to claim 1, wherein the trenches, (Figure 6 the via or opening around #20, 24, & 34), are formed along a network of

arrays such that an array contains a single detection element, (Col. 3 Lines 42-51 teaches a matrix of the elements as shown in Figure 6 and since the claim does not recite a narrower definition of a single detection element and a broader interpretation of this limitation will be read such as the matrix can be used to detect one single photon of energy coming from a source).

11. Referring to claim 10, Shigenaka et al. teaches a structure according to claim 1, wherein the conductive walls, (Figure 6 #21 and 33), are in electrical contact with the layers of semiconductor material, (Figure 6 #31 and 12), by doped zones, (Figures 4 & 6 #25 where it is inherent that transistors do have doped zones), of said layers of semiconductor material, (Figure 6 #31 and 12).

12. Referring to claim 11, Shigenaka et al. teaches a structure according to claim 1, wherein the conductive walls, (Figure 6 #33 and 21), are locally electrically insulated, (Figure 6 transistor #25 electrically insulates the node when the transistor is not turned on), from the detection elements, (Figure 6 #31, 12, 13 & 15), and the common electrode, (Figure 6 #24), to constitute electrical charge storage capacitors, (Figure 4 and 6 #25 where the electrical charge can be stored in the gate dielectric of the transistors and where the claim recites the limitation of electrical charge, which can be read in its broadest reasonable interpretation and can be read as any electrical charge no matter how small).

13. Referring to claim 12, Shigenaka et al. teaches a structure according to claim 1, wherein the means of reflecting the light, (Figure 6 shown by arrows facing #11), are arranged above, (Figure 6 where the device could be flipped upside down), the conductive walls, (Figure 6 #33 and 21 the bottom portion of the electrodes that are directly in contact with the semiconductor layers), in order to reflect the light, (the light will be reflected from the bottom portion of layers

#33 and 21 that are directly connected to the semiconductor layers because it is inherent that metal has a high index of reflectivity), to be detected, directed towards the conductive walls, (Figure 6 #33 and 21), towards the elements, (Figure 6 #31, 12, 13 & 15), adjacent to the conductive walls, (Figure 6 #33 and 21).

14. Referring to claim 13, Shigenaka et al. teaches a structure according to claim 1, wherein said superimposition comprises layers of semiconductor material, (Figure 6 #31, 15, and 12), of different nature, (the layers are formed in different locations, and sizes).

15. Referring to claim 14, Shigenaka et al. teaches a structure according to claim 1, wherein the superimposition comprises n layers of semiconductor material, the thickness of each layer is determined as a function of n wavelength ranges defined from the light spectrum so that the layer of semiconductor material located the nearest to the face for receiving the light absorbs virtually all of a first defined wavelength range, the two layers of semiconductor material located nearest the face for receiving the light absorb virtually all of a second defined wavelength range, and so on until n, the intensities measured by each detection element of a same pixel making it possible to restore, as a function of the absorption coefficients of each layer of semiconductor material, the intensities of each of the n wavelengths received by the pixel, (the claim recites the limitation of n, which can be read in its broadest reasonable interpretation and can be reads as n is equal to 0).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A. Mandala Jr. whose telephone number is (571) 272-1918. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

VAMJ
3/4/07

SUE A. PURVIS
SUPERVISORY PATENT EXAMINER